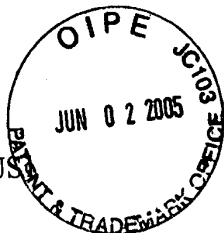


BUR920040040US



IFW

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re patent application of

Anderson, et al.

Serial No. 10/711170

Group Art Unit: Unknown

Filing Date: 8/30/04

Examiner: Unknown

For: FINFET WITH LOW GATE CAPACITANCE AND LOW EXTRINSIC RESISTANCE

Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicants' duty of disclosure under 37 CFR §1.56, applicants respectfully bring the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner. This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicants are aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

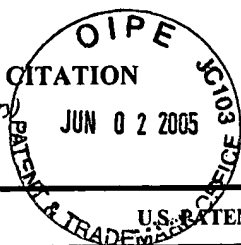
Respectfully submitted,

Mohammad S. Rahman  
Registration No. 43,029

McGinn & Gibb, PLLC  
2568-A Riva Road, Suite 304  
Annapolis, Maryland 21401  
(301) 261-8625  
Customer No. 29154

# INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)



|  |  |
|--|--|
| Docket Number (Optional)<br><b>BUR920040040US1</b> | Application Number<br><b>10/711170</b> |
| Applicant(s)<br><b>Anderson, et al.</b>            |  |
| Filing Date<br><b>8/30/04</b>                      | Group Art Unit<br><b>Unknown</b>       |

## U.S. PATENT DOCUMENTS

| *EXAMINER<br>INITIAL | REF | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE<br>IF APPROPRIATE |
|----------------------|-----|-----------------|------|------|-------|----------|-------------------------------|
|                      |     |                 |      |      |       |          |                               |
|                      |     |                 |      |      |       |          |                               |
|                      |     |                 |      |      |       |          |                               |
|                      |     |                 |      |      |       |          |                               |
|                      |     |                 |      |      |       |          |                               |

## U.S. PATENT APPLICATION PUBLICATIONS

| *EXAMINER<br>INITIAL | REF | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE<br>IF APPROPRIATE |
|----------------------|-----|-----------------|------|------|-------|----------|-------------------------------|
|                      |     |                 |      |      |       |          |                               |
|                      |     |                 |      |      |       |          |                               |
|                      |     |                 |      |      |       |          |                               |
|                      |     |                 |      |      |       |          |                               |

## FOREIGN PATENT DOCUMENTS

|  | REF | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation |    |
|--|-----|-----------------|------|---------|-------|----------|-------------|----|
|  |     |                 |      |         |       |          | YES         | NO |
|  |     |                 |      |         |       |          |             |    |
|  |     |                 |      |         |       |          |             |    |
|  |     |                 |      |         |       |          |             |    |
|  |     |                 |      |         |       |          |             |    |
|  |     |                 |      |         |       |          |             |    |

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

|  |  |   |
|--|--|---|
|  |  | Lindert, et al., "Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process", IEEE Electron Device Letters, Vol. 22, No. 10, October 2001, Pages 487-489 |
|  |  |   |

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.